CLAIMS

1. Method for assembling a first and a second wafer (12, 14, 22, 24), of which at least the first, known as chamfered wafer, has at least a chamfered edge (7, 17), comprising:

- a routing stage of at least one part of the chamfered edge of the first wafer (12, 22);
- then, an assembling stage of the first wafer, routed, and of the second wafer.

2. Method as in claim 1, further comprising, after assembling, a thinning out stage of at least the first wafer, leaving at least a layer (16) on the second wafer.

3. Method for transplanting a layer (16, 28) of material or circuits or components, known as transplant layer, comprising:

- the routing of a first wafer (12, 22) of material, in which the transplant layer is made, at least around or on the periphery of this transplant layer;
- the transplanting of this layer onto a second wafer (14, 24) of material.

4. Method as in claim 3, in which a part of the material of the transplant layer is eliminated during routing.

5. Method as in one of claims 1 to 4, the routing stage being performed over the entire thickness e of the first wafer.

6. Method as in one of claims 1 to 4, the routing stage being performed over a thickness ed less than the thickness e of the first wafer.

7. Method as in claim 6, the routing stage being performed over a thickness ed greater than or equal to a thickness of a layer (16, 28) of the first wafer to be transplanted onto the second wafer.

8. Method as in claim 6, the routing stage being performed over a thickness ed less or equal to a thickness of a layer (16, 28) of the first wafer to be transplanted or transferred onto the second wafer.

9. Method as in one of claims 1 to 8, comprising an additional routing stage after assembling the first and second wafers.

10. Method as in one of claims 1 to 9, the routing stage being performed over a thickness ed of the first wafer of between 1 μm and 100 μm.

11. Method as in one of claims 1 to 10, the fist wafer being chamfered and comprising at least a chamfered edge (5).

12. Method as in claim 11, the routing stage being performed over a width Ld, measured on a plane parallel to that of the first wafer, at least equal to the width L of the chamfered edge, measured on the same plane.

13. Method as in any of claims 1 to 12, the routing stage being performed over a width Ld, measured on a plane parallel to that of the first wafer, at least equal to the width of the zone of this first wafer which can not, without routing, be assembled with the second wafer.

molecular adhesion or via bonding using an adhesive substance.

21. Method as in any of the previous claims, components or circuits (16) having been made in the first wafer before routing.

22. Method as in any of the previous claims, the first wafer previously being covered in a protective layer (18).

23. Method as in the previous claim, the protective layer being eliminated locally, before routing of the first wafer, in a zone located above the zone to be routed of the first wafer.

24. Method as in the previous claim, the local elimination of the protective layer being performed via lithography and etching.

25. Method as in claim 22, the protective layer (18) being eliminated after routing of the first wafer.

26. Method as in any of the previous claims, the routing taking place after a previous surface preparation stage of the first wafer with the purpose of assembling or transplanting.

27. Method as in any of claims 1 to 25, the routing taking place before a previous surface preparation stage of the first wafer with the purpose of assembling or transplanting.

28. Method as in any of the previous claims, the routing being performed via mechanical or chemical or mechano-chemical etching or polishing or via plasma etching or via a combination of at least two of these types of etching.

29. Method as in any of the previous claims, at least one of the two wafers being made in a semiconductor material.

30. Method as in the previous claim, at least one of the two wafers being made in silicon or in a III-V type semiconductor material.

31. Method as in any of claims 1 to 29, at least one of the two wafers being made in Germanium or in Germanium silicide (SiGe) or in a piezoelectric material or in an insulating material.

32. Method as in any of the previous claims, the routing stage being performed in a regular manner around the first wafer.

33. Method as in any of claims 1 to 31, the routing stage being performed in an irregular manner around the first wafer, creating a plane (44).

34. Method as in any of claims 1 to 31 or 33, the routing stage being performed in an irregular manner, creating a marking zone (50 and 51).

35. Method as in claim 34, further comprising a marking stage of the first wafer.